

SINGLE BANK SDRAM TIMINGS

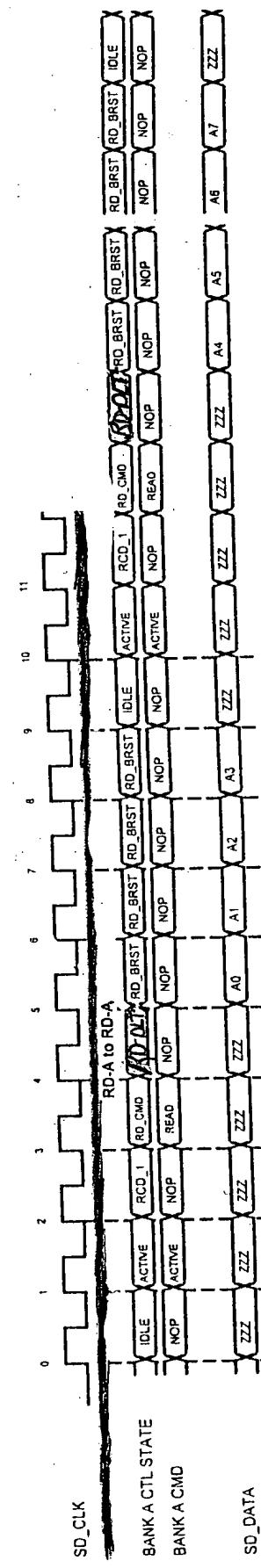
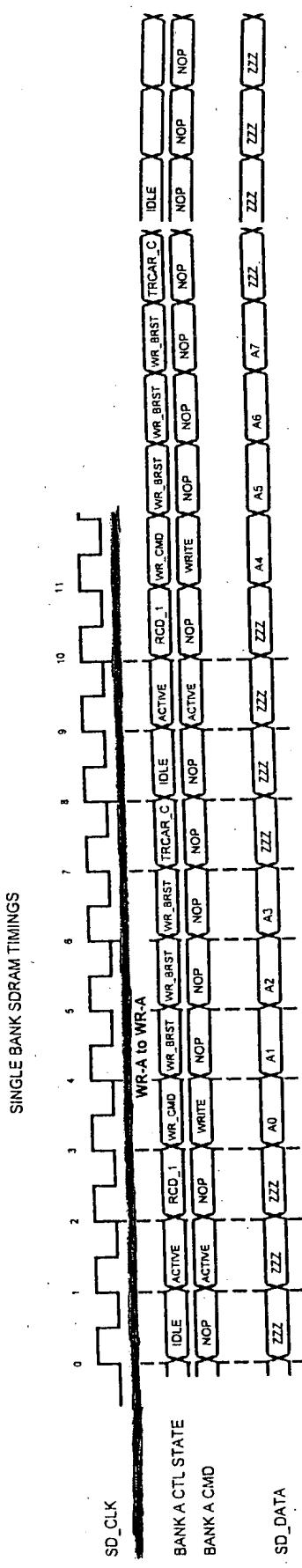


FIG. 15A

BEST AVAILABLE COPY



F/G. 15 D

BEST AVAILABLE COPY

F16. 16D

